REMARKS/ARGUMENTS

This is a response to the Office Action of March 30, 2006, in which a three-month term was set for response. Accordingly, the Applicant includes a request for a one-month extension of time.

Summary of Examiner Interview of July 12, 2006

A telephone interview with the Examiner took place on July 12, 2006 to discuss the prosecution for the subject application. The Examiner discussed the possibility of claim amendments. The Agent for the Applicant explained to the Examiner, by going over a few figures in the subject application, how Applicant's independent claim 34 relates to the Applicant's invention. The Agent for the Applicant then explained how the elements that were cited from the Frey reference (U.S. 6,430,720) differ in structure and function. The Examiner agreed that the elements taught by Frey, which were cited in the Office Action against Applicant's claim 34, are actually different from the Applicant's elements recited in claim 34.

Amendments to the Claims

No amendments have been made to the claims in this current response. No claims have been cancelled or added in this response. Accordingly, there are currently 19 claims pending for this application.

Claim Rejections—35 U.S.C. §102

In paragraph 2 of the Office Action, the Examiner rejected claims 34-36, 44 and 47 under 35 U.S.C. 102(e) as being anticipated by Frey et al. (US 6,430,720), hereinafter referred to as Frey.

Claim 34

In particular, with regard to claim 34, the Examiner is of the opinion that:

> *"Frey et al disclose (Fig. 1) a test circuit (1) for testing an integrated circuit (2) on a wafer the test circuit formed on the wafer with the integrate circuit, the test circuit comprising:*
>
> *A variable ring oscillator circuit including*
>
> *i) a base ring oscillator circuit (18, which includes the delay circuit 70 or 50 in Figs. 3-5, column 12 lines 62-65)*
>
> *ii) a plurality of sub-circuits (2-6) couple to the base ring oscillator circuit (18); and*
>
> *iii) a plurality of switching elements (8, 10) for selectively coupling at least one of the plurality of sub-circuits (2-6) to the base ring oscillator circuit (18); and*
>
> *iv) a control circuit (20) to selectively couple the sub-circuits (2-6) to the base ring oscillator (18) circuit associated with a selected sub-circuit, the test circuit (1) conducts a separate test of the integrated circuit (2) for at least one of the versions of the variable ring oscillator circuit (18)."*

In response, the Applicant respectfully submits that Frey does not teach all of the elements recited in Applicant's claim 34. Firstly, Frey does not teach a plurality of sub-circuits that are selectively coupled to the base ring oscillator. The circuits 2 to 6 in Fig. 1 of Frey that were cited by the Examiner are not selectively coupled to the clock generator circuit 18. Circuit 2 is an internal logic circuit to be tested, circuit 3 exchanges logic states with circuit 2, circuit 4 is a first test register, and circuit 6 is a second test register. Fig. 1 clearly shows that circuits 2 to 6 are not coupled to the clock generator 18. Rather, the clock generator 18 is only coupled to the control circuit 20. Furthermore, circuits 2 to 6 do not appear to have any affect on the clock generator 18, as no feedback exists from any of these circuits to the clock generator 18.

Furthermore, Frey does not teach a control circuit that enables at least one switching element to selectively couple at least one sub-circuit to the base ring oscillator circuit that the Examiner has identified as being circuit 70. Firstly, Fig. 5 in Frey clearly shows that the circuit 70, which is a programmable ring oscillator, is always coupled to circuit elements 74, 84, 86, 92, 94 and 96. Fig. 5 does not show any switches or other elements for selective coupling. Although, Frey teaches the use of multiplexers, these devices cannot be used to selectively couple circuits together, but rather produce an output signal by selecting one of many input signals.

Secondly, Figs. 3 and 4 collectively show the structure of circuit 50 which Frey defines as being the same as circuit 70. Figs. 3 and 4 clearly show that Frey teaches a programmable oscillator comprising a series of buffers always connected to one another in series. The programmable nature of the ring oscillator results from the use of the multiplexers 36 and 64 which are simply used to produce a variable clock output signal based on selecting one of many input signals that are derived from different nodes in the ring oscillator. There are no switches for selectively coupling sub-circuits to the oscillator structure shown in Figs. 3 and 4. The passage from line 58, col. 11 to line 52, col. 12 of Frey discusses this structure in more detail.

Thirdly, the control circuit 20 in Frey that was cited by the Examiner receives a clock signal from the clock generator 18 and does not provide any control inputs to the clock generator 18. Rather, the control circuit 20 only provides test signals LCCK and PHASE to circuits 8 and 2.

Fourthly, the input provided to the clock generator 18 is determined externally by various signals (see Fig. 2). These signals are discussed in Frey in the passage from line 60, col. 9 to line 12, col. 10. These signals include a reset signal RESET (to reset the test circuit), a logic control signal VFCGOFF (to start or stop the clock signal), a logic control signal INVPULSE (to determine the polarity of the clock signal), a control signal DUTYOFF (to control the duty ratio of the clock signal), a first set of control

signals FREQCTR (to control the frequency of the clock signal), and a second set of control signals DUTYCTR (to control duty cycle of the clock signal). It is clear that there aren't any circuits in Frey that provide an input signal to the clock generator 18.

Claim 35

With regards to claim 35, the Examiner is of the opinion that: *"Frey (Fig. 1) discloses the test circuit of claim 34 wherein each test conducted by the test circuit is a parametric test (functional test, see the abstract)".*

In response, the Applicant respectfully submits that Frey only discloses a test circuit that conducts functional (logic only) tests and not parametric tests. For instance, col. 1, lines 33-38 of Frey states: "A method to implement the functional tests is to send logic signals on the inputs (pads or leads) of the circuit to be tested, observing the states of the signals provided on its outputs (pads or leads) and comparing these states with the states theoretically expected. The states of the provided logic signals form what is usually called test patterns or vectors."

In contrast, the Applicant's test circuit is capable of making on chip parametric or measurements. For example, as recited in paragraph [0017] of the subject application, the Applicant teaches that parametric testing takes place by comparing the ratios of the measured oscillation frequencies and the design values of the capacitors to provide an indication of the status of the fabrication process based on original design values.

The Applicant further submits that functional and parametric tests are not the same. A functional test is defined as "*testing that ignores the internal mechanism of a system or component and focuses solely on the outputs generated in response to selected inputs and execution conditions.*" (Institute of Electrical and Electronics Engineers. IEEE Standard Computer Dictionary: A Compilation of IEEE Standard Computer Glossaries. New York, NY: 1990.).

In contrast, parametric testing is defined as "*wafer-level testing of discrete devices such as transistors and resistors.*" (SEMATECH, http://www.sematech.org/publications/dictionary/p_to_ph.htm). Also, from semi.org: "*Parametric tests check the general performance of the device or circuit and ensure that it meets certain input and output voltage, capacitance, and current specifications. Functional tests verify the specified function of the chip; logic chips are put through logic test, while memory chips go through test for data storage and retrieval capabilities. The test equipment at this point consists of computer-controlled probers and handlers for automatic operation of the test process.*" (Semi.org, http://wps2a.semi.org/wps/portal/_pagr/103/_pa.103/248?startRow=1&dFormat=application/msword&docName=P037216).

Accordingly, the Applicant respectfully submits that parametric testing and functional testing are not the same, and it is clear that Frey does not teach or even suggest parametric testing.

Claim 36

With regards to claim 36, the Examiner is of the opinion that: *"Frey (Fig. 1) discloses that the sub-circuits (2-6), when coupled to the base ring oscillator circuit (18), change the frequency of oscillation of the variable ring oscillator circuit".*

In response, the Applicant respectfully submits that circuits 2 to 6 do not affect the frequency of oscillation of the clock generator 18 in Frey. In particular, as can be seen from Fig. 1 of Frey, none of the outputs of circuits 2 to 6 connect to the clock generator circuit 18, and therefore cannot affect the oscillation frequency of the clock generator 18. Furthermore, Fig. 1 in Frey clearly shows that the only inputs to the clock generator 18 are externally provided via input port 22.

Claim 44

With regards to claim 44, the Examiner is of the opinion that: *"Frey (Fig. 1) discloses that the control circuit (20, 3) comprises a sequencer (3) to selectively couple the sub-circuits (2-6) to the variable ring oscillator circuit (18) to produce a series of tests states".*

In response, the Applicant respectfully submits that Frey must load test vectors from external contact probes and clock them in. Then a digital output is recorded into an output register. After this the output register is captured using contact probes and then the actual result is compared with an expected result. See col. 8, lines 15 to 56 in Frey which teach that a primary input 12 provides logic states to the register 4. Furthermore, as explained earlier, Frey does not teach any switches or sub-circuits that can be selectively coupled to a ring oscillator.

In contrast, Applicant's claim 44 recites that sub-circuits are selectively switched into and out of the variable ring oscillator based on the test state signals which are supplied by the sequencer (see paragraph [0113] in the subject application for more information).

Claim 47

With regards to claim 47, the Examiner is of the opinion that: *"Frey (Fig. 1) discloses that the test circuit produces a test result signal that is the output of the variable ring oscillator circuit (18)".*

In response, the Applicant respectfully submits that Frey does not disclose the use of the output of a variable ring oscillator as the test result signal. The passage in column 6, lines 46 to 57 as well as Fig. 1 of Frey clearly show that the test result signal consists of M vectors that are inputted into circuit 6 and may be read at output port 16. The test result signal comes from the output of the circuit 2 that is being tested. Fig. 1 of Frey shows that the output of the clock generator 18 is only provided to a divider 24, and the control circuit 20, and is not used as part of the test results.

In contrast, the Applicant teaches the variable ring oscillator output (34) is coupled to a synchronization element (66) which is coupled to a coupler (68) which is coupled to an antenna (50) which is coupled to the test unit (12). Accordingly, the test result signal is based on the output of the variable ring oscillator.

Claim 50

With regards to claim 50, the Examiner is of the opinion that: *"Frey (Fig. 1) discloses that the control circuit further comprises a second ring oscillator adapted to provide a first clock signal, and a divider (24) coupled to the ring oscillator and the sequencer (3) and adapted to provide a second clock signal (TCK), wherein the second clock signal (TCK) is provided to the sequencer (3) can provide a series of test state signals to the variable ring oscillator circuit (18) and plurality of sub-circuits (2-6)."*

In response, the Applicant respectfully submits that Frey does not teach the elements of claim 50. In particular, Frey's divider 24 does not produce a clock signal that is provided to a sequencer. The clock signal cited by the examiner (TCK of Fig. 1) is an external clock signal (see column 6 lines 33 to 34 of Frey, which refer to TCK as "an external clock signal"). Furthermore, Frey does not disclose a sequencer that provides a series of test state signals to a variable ring oscillator. Circuit 3 of Fig. 1, which the Examiner argues is a sequencer, simply provides additional logic signals for testing circuit 2. Also, circuit 3, is not coupled to an oscillator circuit (see Fig. 1), so even if circuit 3 was a sequencer, which it is not, it cannot be said to provide test state signals to a variable ring oscillator circuit.

Claim Rejections—35 U.S.C. §103(a)

The Examiner has rejected claims 37, 38, 40, 41, 45, 46 and 54-57 under 35 U.S.C. 103(a) as being unpatentable over Frey in view of Merrill et al (US 5,039,602), hereinafter referred to as Merrill. The Examiner also rejected claims 39, 42 and 43

under 35 U.S.C. 103(a) as being unpatentable over Frey in view of Merrill and further in view of Lee (US 5,686,855).

Claims 37, 38, 40, and 41

With respect to claims 37, 38, 40, and 41, the Examiner is of the opinion that: *"Frey discloses everything except for the capacitive load. On the other hand, Merrill disclose (Fig. 2) the test circuit of claim 36 wherein at least one sub-circuit comprises a capacitive load (24) to change the frequency of oscillation of the variable ring oscillator circuit. It would have been obvious to one having an ordinary skill in the art at the time of the invention was made to modify the teaching of Frey and use the capacitive load as taught by Merrill for the purpose of altering the frequency of the test circuit."*

In response, the Applicant respectfully submits that a person of ordinary skill in the art would not combine the Frey and Merrill references. Frey is directed towards functional testing while Merrill is directed towards characterizing A.C. performance of an integrated circuit based on D.C. measurements. These are two totally different applications, and two totally different approaches are taught that are not compatible and cannot be combined.

Furthermore, even if one were to combine the Frey and Merrill circuits, one would still not arrive at the Applicant's claimed invention. Firstly, it is clear that Frey doesn't teach all of the claimed elements of Applicant's claim 34. Secondly, Merrill does not teach using any elements to change the frequency of a ring oscillator. For instance, the capacitor 24 in Merrill, which was cited by the Examiner, does not change the frequency of oscillation of a ring oscillator. Column 5 lines 29-33 of Merrill state: "Converter 34, in combination with an external reference capacitor 24 and parametric tester 26, produces a D.C. voltage, the magnitude of which is directly related to the frequency of the output oscillator 30." Accordingly, the Applicant submits that Merrill teaches using the capacitor 24 to produce a D.C. voltage that is related to the frequency of an oscillator and it is not utilized to affect the frequency of the oscillator.

Claim 45

With respect to claim 45, the Examiner is of the opinion that: *"Frey discloses everything except for the test circuit formed on the wafer. On the other hand, Merrill teaches that the test circuit (22) is formed on the wafer (84) with at least two metallization layers of the IC (86). It would have been obvious to one having an ordinary skill in the art at the time of the inventions was made to modify the teaching of Frey and use test circuit formed within the wafer for the purpose of self testing."*

In response, the Applicant respectfully submits that Frey and Merrill are not combinable. Secondly, the circuits in both Frey and Merrill both require contact. In particular, after the circuits are implemented and the testing stage is complete no further processing, such as front end manufacturing steps, may be performed on the wafer for both Frey and Merrill. Furthermore, the Applicant has reviewed the Merrill reference and found no teaching of using just two metallization layers. The Applicant respectfully requests the Examiner explicitly point out such a teaching.

Claim 46

With respect to claim 46, the Examiner is of the opinion that: *"Frey discloses everything except for different layers. On the other hand, Merrill discloses (Fig. 2) that the test circuit (22) is formed on the wafer (84) with at least one metallization layer of the IC (86) and one polysilicon layer of the IC (86). It would have been obvious to one having an ordinary skill in the art at the time the invention was made to modify the teaching of Frey and use a test circuit formed within the wafer for the purpose self testing."*

In response, the Applicant respectfully submits that the comments made for claim 45 also apply to claim 46. Merrill and Frey are not combinable and do not, alone or in combination, teach all features recited in Applicant's claim 46. Furthermore, the Applicant could not find a teaching in Merrill with regards to the layers recited in Applicant's claim 46.

Claim 54 and 55

With respect to claims 54 and 55, the Examiner is of the opinion that: *"Frey discloses everything except for the test circuit is formed adjacent to a die. On the other hand, Merrill discloses (Fig. 2) the test circuit (22) is formed adjacent to a die containing the IC (86) and on the IC (86). It would have been obvious to one having an ordinary skill in the art at the time of the invention was made to modify the teaching of Frey and use test circuit formed within the wafer for the purpose self testing."*

In response, the Applicant reiterates that Frey and Merrill are not combinable, and do not, alone or in combination, teach all features recited in Applicant's claims 54 and 55. Furthermore, the Applicant submits that Frey requires external inputs and outputs. Accordingly, Frey cannot fit 22 bond pads adjacent to the dies without using additional wafer surface area, which would result in fewer die per wafer and a higher cost per die. In addition, even if one were to combine the two references, the result would be an increase in the size of the integrated circuits and require many transistors and a greater amount of power.

The circuits of the subject application provide a clear economic advantage over the teaching of Frey and Merrill. Part of this advantage comes from the fact that less transistors and therefore less chip real estate is taken up by the Applicant's invention. Therefore, the test circuits of the subject application allow for multiple placements on various wafer locations. Furthermore, less power is consumed by the Applicant's circuit compared to the circuits of Merrill and Frey.

Claim 56 and 57

With respect to claims 56 and 57, the Examiner is of the opinion that: *"Frey discloses everything except for the test circuit being formed on the wafer and near the edge of the wafer. On the other hand, Merrill discloses (Fig. 2) the test circuit (22) is formed adjacent to a die containing the IC (86) and on the IC (86). It would have been obvious*

to one having an ordinary skill in the art at the time of the invention was made to modify the teaching of Frey and use the test circuit formed within the wafer for the purpose self testing."

In response, the Applicant reiterates that Frey and Merrill are not combinable and do not, alone or in combination, teach all features recited in Applicant's claims 56 and 57. Furthermore, the Applicant respectfully submits that it would not be obvious to modify the teaching of Frey to use the circuit for self-testing because the operation of Frey's circuit requires external inputs and outputs. In contrast, certain embodiments disclosed in the subject application may be placed at multiple locations on a wafer without affecting the surface area of an individual die or the total number of die per wafer.

In addition, Frey's circuit requires 22 bond pads which in turn require a large surface area. Furthermore, given that the bond pads must be contacted mechanically, they must include electrostatic discharge protection for each bond pad. This would further increase the required surface area.

Claim 39

With respect to claim 39, the Examiner is of the opinion that: *"Frey (Fig. 1) and Merrill (Fig. 2) disclose everything except for the sub-circuit comprises a delay element to change the frequency of oscillation of the variable ring oscillator circuit. On the other hand, Lee teaches the sub-circuit comprises a delay element (24, 28) to change the frequency of oscillation of the variable ring oscillator circuit. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify the teaching of Frey and Merrill with a delay circuit of Lee for the purpose of alternate the frequency of the signal during the testing process."*

In response, based on comments made above, it is clear that one skilled in the art would not combine the Frey and Merrill references. Furthermore, the Applicant submits that one skilled in the art would not combine the Frey and Lee references. As mentioned

earlier, Frey is directed towards functional testing. Lee is directed towards a process monitor for CMOS integrated circuits. Process Monitoring is defined as "*determination of surface/material characteristics at various stages of device manufacturing sequence; carried out for the purpose of evaluation of process performance; goal: as early as possible detection of process malfunction; the most effective when carried out in-line, in real time.*" (SemiconductorGlossary.com http://semiconductorglossary.com/default.asp?searchterm=process+monitoring and also: http://www.mosis.org/Technical/process-monitor.html). Accordingly, Frey and Lee are directed towards the solution of different problems. Also, it is very clear that they both teach very different circuit implementations that cannot be combined without changing the intended operation of either of the Frey and Lee circuits. Accordingly, the Applicant submits that one skilled in the art would not think to combine all three of these references.

Furthermore, the Applicant respectfully submits that none of the cited references, alone or in combination, teach or even suggest the elements recited in Applicant's claim 39. None of the references teach switching in a delay element. The frequency of Frey's ring oscillator is determined by an external control by selecting a fixed discrete delay. The frequency of Merrill's ring oscillator is simply determined by the number of inverters that are used which is fixed after implementation (see Fig. 3 in Merrill). Furthermore, Lee simply teaches the use of two delay units that are connected somewhat in parallel with some logic circuitry. Lee further teaches using the phase differences between the rising and falling edges of the pulses at the outputs of the first and second delay units to determine the performance of an integrated circuit.

In contrast, the Applicant's claim recites a situation where the circuit under test is part of the delay element of the ring oscillator, hence the circuit under test influences the ring oscillator frequency and thus the test result. None of the cited references provide for this influencing the delay of a ring oscillator in this manner.

Claims 42 and 43

With regards to claims 42 and 43, the Examiner is of the opinion that: "Lee discloses that the delay element (24, 28) comprises at least one inverter which is CMOS inverter".

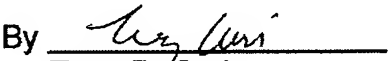
In response, the Applicant respectfully submits that the cited references are not combinable, and that, either alone, or in combination, do not teach all of the Applicant's claimed elements.

CONCLUSION

Based on the above comments, the Applicant respectfully submits that claims 34-47, 50, and 54-57 are novel and inventive over the cited references and should be allowed. Accordingly, it is respectfully submitted that the application is now in condition for allowance. If the Examiner has any concerns regarding this response, the Examiner is respectfully requested to contact the undersigned at 416-957-1603.

Respectfully submitted,

BRIAN H. MOORE

By 
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